REMARKS

This Amendment is in response to the Office Action dated August 26, 2004. Claims 1-10 are pending in the present application. Claims 1-10 are rejected. Claims 1 and 6 have been amended to include the limitations of claims 2 and 7 respectively. Claims 3 and 9 have been amended to provide proper dependency. Accordingly, claims 1, 3-6 and 8-10 remain pending in the present application.

Applicant includes a Petition for Extension of Time to extend the deadline for filing a response by one (1) month from November 26, 2004 to December 26, 2004.

Drawing Objections

The Examiner states,

> **1. The drawings are objected to because:**
> **Figure 1, element 100 should be labeled "Second Order Low Pass Filter" or "Second Order LPF".**

Applicant has made this change in accordance with Examiner's request.

> **Figures 2 and 6, elements 206 and the like element (No number in figure 6) should be removed? The requirement to remove elements, such as element 206 in figure 2, is because the outputs of element 204 are directly connected to the inputs of element 208. The presence of element 206 is redundant and confusing.**

Applicant submits that lines across are essentially resistance therebetween element 206 to 204 and is in accordance with transconductor theory. However, to minimize confusion for the Examiner Applicant submits new Figures 2 and 6 which remove the lines.

Disclosure Objections

The Examiner states,

2. The disclosure is objected to because the configuration is confusing. As the examiner has mentioned in the objection to the drawing, element 206 in figure 2 (Similar element is in figure 6) becomes redundant since the direct connection (The lines across 206 from outputs of element 204 to inputs of element 208) would bypass element 206 (No current or signal would go into the element 206).

Appropriate correction is required.

Applicant submits that lines across are essentially resistance therebetween element 206 to 204 and is in accordance with transconductor theory. However, to minimize confusion for the Examiner Applicant submits new Figures 2 and 6 which remove the lines.

Claim Rejections – 35 USC 102

The Examiner states,

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 1232(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Hatcher (US 2002/0160740A1).

Regarding claim 1, Hatcher et al. discloses a method comprising the steps of (figure 3) generating a test signal (C+, C-); and suppressing even-order harmonics due to transistor mismatches (Page 4, entire right columns; page 5, entire left column) within the plurality of transconductor cells (Q1-Q6).

Regarding claim 5, Hatcher et al. discloses the test signal comprises a sinusoidal signal (The RF signal is sinusoidal signal).

Claim Rejections – 35 USC 103

The Examiner states,

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action.

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. Claims 2-4, 6-10, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatcher et al. (US 2002/0160740A1).

Regarding claims 2, 3, 6, 78, Hatcher discloses a system comprising (Figure 3) a plurality of transconductor cells (Q1-Q6); and a signal processor (210) for generating a test signal (328, 332) to the device (204) and for suppressing even order harmonics due to transistor mismatches within the plurality of transconductor cells (Page 4, entire right column; page 5, left column, lines 26-42).

The only difference between Hatcher et al. and the invention claimed is that the claim recites a digital signal processor in place of processor (210).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a digital signal processor into the system of Hatcher et al. because the DC offset to suppress even order harmonic in the bipolar junction transistor (BJT or Analog) as taught by Hatcher et al. (Page 5, Entire left column) would have been obvious for the use of a digital to suppress the even order harmonic in the CMOS (Digital) since Hatcher et al. taught that DC offset compensator allows the DC offset associated with the even order non-linearity in each individual Gilbert cell to be compensated (Page 5, left column, lines 39-42).

Regarding claims 4, 8, 9, the only difference between Hatcher and the invention claim is that the claim recites a second order low pass filter in place of a mixer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the second order low pass filter into the system of Hatcher because adjusting the Dc offset of the second order low pass filter or any electronic device including the mixer of Hatcher having second order harmonic due to transistors mismatch, the even order non-linearity would be compensated (Page 5, left column, lines 39-42).

Regarding claim 10, Hatcher et al. discloses the test signal comprises a sinusoidal signal (The RF signal in sinusoidal signal).

Applicant respectfully traverses these rejections.

Present Invention

A method for calibrating a low pass filter is disclosed. The low pass filter comprises a plurality of transconductor cells. The method comprises generating a test signal to the low pass filter and suppressing even-order harmonics due to transistor mismatches within the plurality of transconductor cells. The suppression is accomplished by introducing an offset voltage on an amplifier in the plurality of transconductor cells that control the drain to source voltage of the input transistors of the cells. By adding a small number of transistors, the mismatch-induced even order harmonics can be greatly reduced. Even-order harmonics are minimized through the application of a control voltage. A method for calibrating against transistor mismatch utilizing a CMOS transconductor that is based on the regulated cascode topology is disclosed. The method is designed to provide suppression of the even-order harmonics, a very small increase in power and a silicon area of the transconductor cell. A well-defined offset is provided by biasing one of the mismatched transistors.

Applicant has amended claims 1 and 6 to incorporate the limitations of claims 2 and 7, respectively. There are no teachings within Hatcher of introducing an offset voltage on an amplifier in the plurality of transconductor cells that control the drain to source voltage of the input transistors of the cells as recited in both of the claims. In so doing the performance of a device that uses this feature is significantly improved. Hatcher does not teach or suggest such a feature in conjunction with the remaining elements of the independent claims 1 and 6. Furthermore, claims 3-5 and 8-10 are allowable claims since they depend from allowable base claims.

The cited references are no more relevant to the present invention than the applied reference.

In view of the foregoing, Applicant's attorney believes that this application is in condition for allowance. Accordingly Applicant respectfully requests reconsideration and allowance of claims 1, 3 and 6 and 8-10 as now presented. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

December 27, 2004

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Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 1, 2 and 6 and replacement sheets for Figures 1, 2 and 6. These sheets replace the original sheets for Figures 1, 2 and 6.

Attachment: 3 Sheets showing changes to Figures 1, 2 and 6.